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EXAMINER	
SHERMAN, STEPHEN G	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/785,099	CHEN, CHING-CHUAN	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Park (US 2004/0119673).

Regarding claim 1, Park discloses a liquid crystal display device comprising:

a plurality of gate lines formed in parallel to each other (Figure 2, GL1, Gli-1,...GLn.);

a plurality of source lines formed in parallel to each other and orthogonal to the gate lines (Figure 2, DL1, DL2,...DLm/2.);

an array of cells formed in rows and columns, each of the cells being formed near an intersection of one of the gate lines and one of the source lines (Figure 2 shows cells 10, 12, 14 and 16 are formed at the intersection of the gate and data lines as explained in paragraph [0074].);

a first transistor of each of the cells disposed at an N-th row and M-th column, N and M being integers, driven by an (N-2)-th gate line (Figure 2 shows that TFT4 of each cell is disposed at an N-th row and M-th column and is driven by the N-2-th gate line.); and

a second transistor of the each of the cells driven by an N-th gate line (Figure 2 shows that TFT3 of each cell is driven by the N-th gate line.).

Regarding claim 16, this claim is rejected under the same rationale as claim 1.

3. Claim 8 is rejected under 35 U.S.C. 102(e) as being anticipated by Martin (US 7,109,958).

Regarding claim 8, Martin discloses a liquid crystal display device comprising:

a plurality of gate lines formed in parallel to each other (Figure 4 shows gate lines Gate 1 through Gate 4.);

a plurality of source lines formed in parallel to each other and orthogonal to the gate lines (Figure 4 shows source lines Data 1 through Data 4.); and

an array of cells formed in rows and columns, each of the cells disposed near an intersection of an N-th gate line and an M-th source line (Figure 4 shows that near the intersection of Gate 3 and Data 3 a cell is formed containing sub-pixels 18 and 20.), N and M being integers, further comprising:

a first capacitor formed between an electrode and an (N-2)-th gate line (Figure 4 shows that capacitor 46 is formed between the pixel electrode and Gate 1.); and

a second capacitor formed between the electrode and an (N-1)-th gate line (Figure 4 shows that capacitor 58 is formed between the pixel electrode and Gate 2).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 2-4 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park (US 2004/0119673) in view of Martin (US 7,109,958).

Regarding claim 2, Park discloses the device of claim 1.

Park fails to teach wherein each of the cells further comprises a capacitor formed between an electrode and the (N-2)-th gate line.

Martin discloses wherein each cell formed near an intersection of one of the gate lines and one of the source lines comprises a capacitor formed between an electrode and the (N-2)-th gate line (Figure 4 shows capacitor 46 formed between a pixel electrode and Gate1.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to for the display cell taught by Park to have a capacitor as taught by Martin in order to sustain the data voltage charged into the liquid crystal capacitors until the next data voltage is charged.

Regarding claim 3, Park discloses the device of claim 1.

Park fails to teach wherein each of the cells further comprises a capacitor formed between an electrode and an (N-1)-th gate line.

Martin discloses wherein each cell formed near an intersection of one of the gate lines and one of the source lines comprises a capacitor formed between an electrode and the (N-1)-th gate line (Figure 4 shows capacitor 58 formed between a pixel electrode and Gate2.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to for the display cell taught by Park to have a capacitor as taught by Martin in order to sustain the data voltage charged into the liquid crystal capacitors until the next data voltage is charged.

Regarding claim 4, Park discloses the device of claim 1.

Park fails to teach wherein each of the cells further comprising a first capacitor formed between an electrode and the (N-2)-th gate line, and a second capacitor formed between the electrode and an (N-1)-th gate line.

Martin discloses wherein each cell formed near an intersection of one of the gate lines and one of the source lines comprises a first capacitor formed between an electrode and the (N-2)-th gate line (Figure 4 shows capacitor 46 formed between a pixel electrode and Gate2.), and a second capacitor formed between an electrode and the (N-1)-th gate line (Figure 4 shows capacitor 58 formed between a pixel electrode and Gate2.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to for the display cell taught by Park to have a capacitor as taught by Martin in order to sustain the data voltage charged into the liquid crystal capacitors until the next data voltage is charged.

Regarding claim 17, this claim is rejected under the same rationale as claim 4.

7. Claims 5-7 and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park (US 2004/0119673) in view of Martin (US 7,109,958) and further in view of AAPA (Figures 2A-2C and page 4, paragraph [006] of the specification).

Regarding claim 5, Park and Martin disclose the device of claim 4.

Park and Martin fail to teach the first capacitor being charged to a first voltage level in response to a fist state of a signal transmitted on the (N-2)-th gate line, and being discharged to a second voltage level in response to a second state of the signal transmitted on the (N-2)-th gate line.

AAPA discloses of a capacitor being charged to a first voltage level in response to a fist state of a signal transmitted on the gate line it is connected to, and being discharged to a second voltage level in response to a second state of the signal transmitted on the gate line it is connected to (Paragraph [006] explains from lines 1-6 that when the gate line connected to the storage capacitor 36 is selected that the voltage is pulled high, i.e. first voltage, and when the selection period ends the capacitor 36 is pulled to the logically low state, i.e. second voltage.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the idea of charging and discharging a capacitor through a previous gate line as taught by AAPA with the capacitor configuration as taught by the combination of Park and Martin such that capacitor 46 would be charged and discharged when the gate line Gate1 is selected then unselected in order to

Regarding claim 6, Park, Martin and AAPA disclose the device of claim 5.

AAPA also discloses of an electrical potential at an electrode being pulled up to a third voltage level in response to a first state of a signal transmitted on the (N-1)-th gate line, and being pulled down to the second voltage level in response to a second state of

the signal transmitted on the (N-1)-th gate line (Paragraph [006] explains from lines 1-6 that when the gate line connected to the node 34-6 is selected that the voltage is pulled high, i.e. third voltage, and when the selection period ends the node 34-6 is pulled to the logically low state, i.e. second voltage.).

Regarding claim 7, Park, Martin and AAPA disclose the device of claim 6.

AAPA also disclose the first capacitor being charged from the second voltage level to the first voltage level in response to a first state of a signal transmitted on the N-th gate line (Paragraph [006] explains from lines 6-9 that that storage capacitor 36 is charged from the negative voltage value, i.e. second voltage level, to the peak value of the source signal line.).

Regarding claim 18, this claim is rejected under the same rationale as claim 12.

Regarding claim 19, this claim is rejected under the same rationale as claim 13.

Regarding claim 20, this claim is rejected under the same rationale as claim 14

Regarding claim 21, this claim is rejected under the same rationale as claim 15.

8. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin (US 7,109,958) in view of Park (US 2004/0119673).

Regarding claim 9, Martin discloses the device of claim 8.

Martin fails to teach of the device further comprising a first transistor including a gate coupled to the (N-2)-th gate line, and a second transistor including a gate coupled to the N-th gate line.

Park discloses of an array of cells formed in rows and columns, each of the cells disposed near an intersection of an N-th gate line and an M-th source line (Figure 2 shows cells 10, 12, 14 and 16 are formed at the intersection of the gate and data lines as explained in paragraph [0074].) further comprising

a first transistor including a gate coupled to the (N-2)-th gate line (Figure 2 shows that TFT4 of each cell is disposed at an N-th row and M-th column and is driven by the N-2-th gate line.), and

a second transistor including a gate coupled to the N-th gate line (Figure 2 shows that TFT3 of each cell is driven by the N-th gate line.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the transistor configuration taught by Park with the display cell structure taught by Martin in order to allow for an image of uniform picture quality to be displayed even when adjacent cells are not charged with a uniform voltage.

Regarding claim 10, Martin and Park disclose the device of claim 9.

Park also discloses the first transistor further comprising a first terminal coupled to the electrode, and a second terminal coupled to the M-th source line (Figure 2 shows

that TFT4 had one terminal connect to the source line DL1 and another terminal that is connected to the pixel electrode.).

Regarding claim 11, Martin and Park disclose the device of claim 9.

Park also discloses the second transistor further comprising a first terminal coupled to the electrode, and a second terminal coupled to the M-th source line (Figure 2 shows that TFT3 has one terminal connected to DL1 and a second terminal connected to the pixel electrode through TFT.).

9. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin (US 7,109,958) in view of Park (US 2004/0119673) and further in view of AAPA (Figures 2A-2C and page 4, paragraph [006] of the specification).

Regarding claim 12, Martin and Park disclose the device of claim 8.

Martin and Park fail to teach wherein a signal transmitted on the M-th source line includes a first voltage level and a second voltage level.

AAPA discloses wherein a signal transmitted on the M-th source line includes a first voltage level and a second voltage level (Figure 2C shows that V(Sm) includes a first and second voltage level.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to make the source signal taught by the combination of

Martin and Park have a first and second voltage level as taught by the AAPA in order to allow for the device to be driven using line inversion or dot inversion.

Regarding claim 13, Martin, Park and AAPA disclose the device of claim 12.

AAPA also discloses the first capacitor being charged to a third voltage level between the first and second voltage levels after a selection period of the previous gate line (Figure 2B illustrates that the voltage of V36 is between the high and low of V(Sm), therefore when this is applied to the configuration taught by the combination of Martin and Park, the first capacitor connected to the N-2-th gate line would be charged as such.).

Regarding claim 14, Martin, Park and AAPA disclose the device of claim 12.

AAPA also discloses an electrical potential of the electrode being kept at a third voltage level between the first and second voltage levels after a selection period of the (N-1)-th gate line (Figure 2B shows that after the selection of V(Gn-1) that potential of the electrode shown as V36 is held at a voltage between o and 10 volts starting at approximately 37.5μs.).

Regarding claim 15, Martin, Park and AAPA disclose the device of claim 12.

AAPA also discloses the first capacitor being charged to the first voltage level after a selection period of the N-th gate line from a third voltage level between the first and second voltage levels (Figure 2C shows that after selection of Gn which occurs

approximately at 25μs in Figure 2B that V36 reaches the first potential of 10V which is the same as the first voltage value of V(Sm).).

10. Claims 22-23 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin (US 7,109,958) in view of AAPA (Figures 2A-2C and page 4, paragraph [006] of the specification).

Regarding claim 22, please refer to the rejection of claim 8, and furthermore Martin also discloses of selecting an (N-2)-th gate line, selecting an (N-1)-th gate line, and selecting the N-th gate line (Figure 5 shows that Gate 1 is selected and Gate2 is selected, where Gate1 is the (N-2)-th gate line from gate line Gate3 and Gate2 is the (N-1)-th gate line form gate line Gate3. Figure 5 also shows that Gate3 is selected.).

Martin fail to teach that the method includes providing a signal including a first voltage level and a second voltage level from the M-th source lines; charging a first capacitor of the each of the cells to a third voltage level between the first and second voltage levels after a selection period of the (N-2)-th gate line; keeping an electrical potential of a terminal of the first capacitor at the third voltage level after a selection period of the (N-1)-th gate line; and charging the first capacitor to the first voltage level after a selection period of the N-th gate line from the third voltage level.

AAPA discloses of a method comprising:

providing a signal including a first voltage level and a second voltage level from the M-th source lines (Figure 2C shows that V(Sm) includes a first and second voltage level.);

charging a first capacitor of the each of the cells to a third voltage level between the first and second voltage levels after a selection period of a previous gate line (Figure 2B illustrates that the voltage of V36 is between the high and low of V(Sm), therefore when this is applied to the configuration taught by the combination of Martin and Park, the first capacitor connected to the N-2-th gate line would be charged as such.);

keeping an electrical potential of a terminal of the first capacitor at the third voltage level after a selection period of the (N-1)-th gate line (Figure 2B shows that after the selection of V(Gn-1) that potential of the electrode shown as V36 is held at a voltage between o and 10 volts starting at approximately 37.5μs.);

charging the first capacitor to the first voltage level after a selection period of the N-th gate line from the third voltage level (Figure 2C shows that after selection of Gn which occurs approximately at 25μs in Figure 2B that V36 reaches the first potential of 10V which is the same as the first voltage value of V(Sm).).

Regarding claim 23, Martin and AAPA disclose the method of claim 22.

AAPA also discloses a method further comprising forming a first transistor and a second transistor in the each of the cells (Figure 2A shows transistors 34 and 38.).

Regarding claim 25, Martin and AAPA disclose the method of claim 23.

AAPA also discloses a method further comprising driving the second transistor through the N-th gate line (Figure 2A shows that transistor 34 is driven through gate line Gn).

11. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Martin (US 7,109,958) in view of AAPA (Figures 2A-2C and page 4, paragraph [006] of the specification) and further in view of Park (US 2004/0119673).

Regarding claim 24, Martin and AAPA disclose the method of claim 23.

Martin and AAPA fail to teach that the method further comprises driving the first transistor through the (N-2) gate line.

Park discloses a method comprising driving a first transistor through the (N-2) gate line (Figure 2 shows that TFT4 is driven by the N-2-th gate line.)

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the transistor configuration taught by Park with the display cell structure taught by Martin in order to allow for an image of uniform picture quality to be displayed even when adjacent cells are not charged with a uniform voltage.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kwon et al. (US 2004/0135751) discloses of a method and apparatus of driving a liquid crystal display device where two TFTs disposed in a cell are both driven by either even or odd gate lines, where one is driven by an N-th gate line and the other is driven by the N-2-th gate line.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

15 November 2006

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SUPERVISORY PATENT EXAMINER